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High-performance all-printed amorphous oxide FETs and logics with electronically compatible electrode/ channel interface

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ABSTRACT

Oxide semiconductors typically show superior device performance compared to amorphous silicon or organic counterparts, especially, when they are physical vapor deposited. However, it is not easy to reproduce identical device characteristics when the oxide field-effect transistors (FETs) are solution-processed/ printed; the level of complexity further intensifies with the need to print the passive elements as well. Here, we developed a protocol for designing the most electronically compatible electrode/ channel interface based on the judicious material selection. Exploiting this newly developed fabrication schemes, we are now able to demonstrate high-performance all-printed FETs and logic circuits using amorphous indium-gallium-zinc oxide (a-IGZO) semiconductor, indium tin oxide (ITO) as electrodes and composite solid polymer electrolyte as the gate insulator. Interestingly, all-printed FETs demonstrate an optimal electrical performance in terms of threshold voltages and device mobility and may very well be compared with devices fabricated using sputtered ITO electrodes. This observation originates from the selection of electrode/ channel materials from the same transparent semiconductor oxide family, resulting in the formation of In-Sn-Zn-O

(ITZO) based diffused a-IGZO/ ITO interface that controls doping density while ensuring high electrical performance. Compressive spectroscopic studies reveal that Sn doping mediated excellent band alignment of IGZO with ITO electrodes is responsible for the excellent device performance observed. All-printed *n*-MOS based logic circuits have also been demonstrated towards new-generation portable electronics.

Keywords: *ink-jet, all-printed, amorphous In-Ga-ZnO, electrolyte gating, FET and logic*

■ INTRODUCTION

Solution processing, easy fabrication, large area compatibility, cost effectiveness along with integration flexibility and stretchability are becoming the driving factors for the scientific community to carry out research in oxide-based next generation smart electronics.[1–4] In this context, the amorphous oxide semiconductors are becoming the most attractive choice as they possess an exceptional combination of properties that include high electronic performance, transparency, spatial homogeneity and somewhat superior mechanical properties than their crystalline oxide semiconductor counterparts.[5–9] However, their electronic performance is found to deteoriate once these materials are solution processed or printed as compared to when they are fabricated using physical vapor deposition (PVD) techniques.[10–12] Here, the motivation behind printing electronic circuitry is to enable a cost effective and easy fabrication route for large area and bulk volume of use-and-throw type consumer electronics.[13–19] However, it requires a wide range of scientific and technical knowledge in order to address various fundamental issues related to the printing processes, such as, the development of printing compatible materials, preparation of high quality inks, compliance of the prepared ink to the host substrate, when necessary additional surface treatment of the host substrates, process optimization for each printing components and so on.[20] However, it is to

be noted that the full potential of this technology may only be exploited when each and every component of a circuitry would be printed. Several attempts have been made in the recent times, where ink-jet printed semiconductor oxides have been used as the channel layer of fabricated FETs.[21–23] Among which few reports have even demonstrated complete room temperature fabrication of printed devices showing its potential in additive manufacturing techniques on inexpensive and flexible substrates.[22] However, in most of the previous attempts, only the channel layer has been printed, whereas the rest of device components have been fabricated using various high-cost alternatives (e.g. different PVD techniques).[24–28] Therefore, it can be stated that in this ongoing quest of printed logic electronics, the primary focus has always been concentrated around optimizing the superior quality of active materials. The passive components of the FETs are often forgotten. Interestingly, the scenario may completely change if each and every component of a device is printed. Understandably, it is indeed difficult to print the passive structures with narrow channel lengths, and in addition, due to the spatial inhomogeneity and high roughness resulting from the printed coarse-grained inorganic semiconductor layer, the channel length sensitivity may become a matter of concern for the all-prinetd long-channel thin film transistors (TFTs). Recently, as a rare example of all-printed TFTs, Scheideler *et al.* have demonstrated low temperature (≤ 250 ºC) fabrication of FETs by printing an aqueous ink based aluminum doped cadmium oxide as source/ drain (S-D) electrodes and indium oxide as the channel element.[23]

In this context, here we show that high-performance all-printed devices can be realized using a-IGZO as the channel layer, in combination with precursor derived printed transparent conducting oxide electrodes, such as ITO with an excellent band alignment at the S-D/ channel interface, resulting in near Ohmic contacts. It is again non-trivial to obtain an easy-to-print high-performance dielectric. In the present study, a composite solid polymer electrolyte (CSPE) as an electronic insulator has been used, which is at the same time easy-to-print, non-toxic and can show adequate thermal and environmental compatibility.[21,29,30] On the other

hand, the very high capacitance (1-10 μF/cm^2) of the electrolytes significantly reduces the operation voltage requirement down to 1-2 volts and makes the devices completely battery compatible and suitable for portable electronic applications.

In case of all-printed devices, the selection of material is quite crucial; mimicking the approach of modern Si-technology, where heavily doped silicon is used as the drive electrodes, here we have chosen ITO, which is a heavily doped transparent conducting oxide (TCO), as the electrode material. Such a selection from the similar material family with maximum possible common constituents may right-away provide an opportunity to have a superior electronically compatible interface (especially, when all the device components are solution processed/ printed), by self-organizing or re-structuring atoms at the interface region. Furthermore, in order to facilitate mixing of atoms of individual layers at the interface, same solvents have been used during the preparation of the precursor inks. It may be noted that the selection of ITO as the passive electrodes is certainly not new, however, here we would like to take full advantage of ITO as the electrode material by forming a electronically compatible diffused interface layer upon annealing. Although usually not practiced, the effect of the intentional intermixing of atoms at the metal/ semiconductor interface is found to be beneficial in the present study to control carrier density at the channel layer ensuring channel conductance at zero gate, at the same time, ensuring high device performance, in terms of field-effect mobility. Finally, we also demonstrate and compare all-printed *n*-MOS based inverters with various load conditions.

■ EXPERIMENTAL SECTION

Ink Preparation. IGZO: A 0.1 M parent solutions of $In(NO_3)_3 \cdot xH_2O$, $Ga(NO_3)_3 \cdot xH_2O$ and $Zn(CH_3COO)_2 \cdot 2H_2O$ are prepared separately using the mixture of 2-methoxyethanol and ethylene glycol organic solvents with a volume ratio of 8:2, respectively.

The appropriate volumes of these parent solutions are mixed in an atomic ratio of In: Ga: Zn = 63:7:30 and continuously stirred for one hour to prepare a clear transparent precursor ink for IGZO. ITO: Indium nitrate hydrate (99.9 %,) and tin(IV) chloride pentahydrate (99.9 %,) are separately dissolved in 2-methoxyethanol. These solutions are mixed in the cation ratio of In: Sn = 9:1 and stirred for one hour to prepare a clear transparent precursor ink for ITO. Composite Solid Polymer Electrolyte (CSPE): The electrolyte is obtained by stirring the clear solution of 0.3 g PVA in 6 g of DMSO together with a solution of 0.07 g $LiClO_4$ in 0.63 g PC. The stirring is carried out overnight (~12 hours) in order to properly homogenize the electrolyte ink.

Device Fabrication. All devices are fabricated on cleaned SiO_2/Si substrate. SiO_2/Si substrate is cleaned using standard piranha treatment (i.e. submersing in 3:1 volume ratio of H_2SO_4 and H_2O_2 for 10 minutes). After cleaning, substrates are washed thoroughly with a copious amount of DI water and dried just before the use. The all-printed FETs are fabricated with the printing of ITO ink as two parallel lines (S-D electrodes) and an equidistant rectangle (G electrode in the displaced/in-plane geometry) as shown schematically in the Figure 1a. Subsequently, the ITO-based printed coplanar passive structure is dried at 130 ℃ for 30 minutes on a hot plate in ambient air. Next, the semiconducting IGZO layer has been printed to bridge the S-D electrodes and subsequently dried at 130 ℃ for 30 minutes. At this stage, the printed devices are annealed at 400, 450 and 500 ℃ for 1 hour through one-step heating. In order to comprehend the effect of one-step heating, the devices are also prepared with two separate steps annealing, one annealing step for printed ITO (at 500 ℃) and the other for printed a-IGZO (at 400 ℃). The devices with lithographically patterned sputtered ITO electrodes and printed a-IGZO (annealed at 400 ℃ and 500 ℃) have also been fabricated for comparison purpose. At the last step, the fabrication of FET is completed with the printing of CSPE gate insulator layer that cover the a-IGZO channel completely and the ITO gate

electrode partially (see Figure 1a for complete fabrication steps). The channel length and width of the devices with sputtered ITO passives were stricktly maintened at 50 and 100 μm, respectively; for the all-printed FETs, owing to limited accuracy of the printing process itself, the device dimensions may have varied by ± 10 μm, however, high resolution optical images were used in each case to ascertain the channel dimentions, which would later be used for the mobility calculations. For the capacitance measurement, two in-plane parallel electrodes test structures were fabricated and CSPE was printed to cover both the terminals. One terminal was composed of lithographically patterened sputtered ITO, while the other was printed and annealed a-IGZO.

■ RESULTS AND DISCUSSIONS

Figure 1a shows the complete fabrication steps of the all-printed FETs in a sequential manner. Source (S), drain (D) and gate (G) electrodes were printed on a cleaned SiO_2/ Si substrate using ITO precursor based ink. After the ITO ink is dried, the IGZO precursor ink was printed to form the semiconductor channel layer and subsequently dried. These printed structures are then annealed through either one-step or two-steps annealing processes and finally the CSPE layer is printed to cover the channel region completely and the gate electrode partially. The thickness of printed ITO and IGZO has been measured by profilometer and estimated to be 150 nm and 70 nm, respectively. Prior to the electrical measurements, systematic structural and morphological characterizations of the annealed ITO and IGZO layers have been carried out at different temperatures. The XRD patterns of ITO and IGZO layers, spin-coated onto SiO_2/ Si substrates and subsequently annealed at ~400, 450 and 500 °C temperatures are shown in Figures 1b and 1c, respectively. The annealing transforms the ITO precursor into a polycrystalline phase, whereas the IGZO remains amorphous in nature. The XRD patterns of annealed ITO layers exhibit characteristic peaks at 13.97°,

16.14°, 22.93° and 26.93°, which correspond to (222), (400), (431) and (440) reflections of cubic structure of In_2O_3, respectively. The crystallite size of ITO annealed at 400, 450 and 500 °C has been calculated using Debye-Scherrer equation from the full-width at half-maximum of (222) peak and found to be 15.9, 16.3 and 17.1 nm, respectively. The atomic force microscopy (AFM) images of ITO and a-IGZO were recorded on real FET device annealed at 400 °C which is shown in Figures 1d and 1e, respectively. The root mean square value of roughness (R_{rms}) for ITO was found to be 5.8 nm, however, in comparison, the R_{rms} value for a-IGZO was estimated to be much smaller, 0.25 nm only, which is typically the case for predominantly amorphous films; in absence of granular crystalline phases, the surface appears extremely smooth and homogeneous. In the present study, the solution processed ITO ink has been printed as electrodes in fabricating the FETs, hence, it is believed to be important to compare the sheet resistance of solution procesaable ITO with the commercially available sputtered ITO of comparable thickness (both around 150 nm). The sheet resistance has been measured using van der Pauw geometry in both cases and its variation for spin-coated ITO precursor ink with respect to annealing temperatures is shown in Figure S1. The sheet resistance of solution processed ITO films is found to be 1.5×10^4 Ω/□ at 400 °C and it decreased down to 2.5×10^3 Ω/□ at 500 °C annealing temperature. The decrease in measured sheet resistance may primarily be related to a relatively superior densification and low porosity/ structural defects in the higher temperature annealed films. These sheet resistance values compare reasonably with the earlier reports, however, it is substantially higher as compared to the commercially available sputtered ITO which typically shows a sheet resistance value of only 15 Ω/□, about two orders of magnitude lower than the solution-processed films. Here, the high sheet resistance value of the solution processed ITO can be attributed to the large degree of structural defects, micro-cracks, porosity and low density of grains as compared to the physical vapor deposited films. While, a substantial decrease in resistance may be possible when the solution derived films are annealed in special reducing

atmosphere,[31,32] such practices are not suitable for device fabrication, especially, when performing one-step annealing along with the semiconductor layer.

The transfer and output characteristics of the all-printed FETs for one-step annealing at different temperatures are shown in Figure 2. The transfer curves are presented in Figure 2a, c, and e for 400, 450 and 500 °C annealing temperatures, respectively, for a constant drain to source voltage (V_{DS}) of 1.0 V. The FETs show good device performance within the low operating voltage range (± 1.0 V) due to the high capacitance of the CSPE insulator. The output characteristics are presented at different V_{GS} in Figure 2b, d and f for 400, 450 and 500 °C annealed devices, respectively. The output characteristics show a linear behavior at low V_{DS} region, thereby ensuring near Ohmic S-D (ITO)/ channel (a-IGZO) interface. While, the saturation behavior for higher V_{DS} indicates a complete pinch-off of the channel, occasionally a slight decrease in the saturation current has been observed, which can be attributed to the negative differential resistance (NDR) effect.[33] It can be noticed that all the devices including the 400 ºC annealed ones have shown good switching behavior. However, at 400 ºC annealing, the resistance of ITO is found to be four orders higher than the sputtered ITO (Figure S1), as a result, at this temperature the on current (I_{on}) seems to be limited largely by the printed ITO passives. This is apparent with sudden saturation of drain current ($I_{D,sat}$) after 0.5 V V_{GS} (Figure 2a). Hence, a large increase in $I_{D,sat}$ has been recorded for devices annealed at higher temperatures (Figure 2c and e). Furthermore, the on/off current ratio ($I_{on/off}$) has also been found to increase for 450 and 500 °C annealed devices as compared to the 400 °C annealed ones, (Table 1), whereas the threshold voltage (V_T) and subthreshold swing (SS) values are calculated to be almost identical, around 0 ± 0.1 V and 100 ± 10 mV decade^{-1}, respectively. It is to be noted that these extracted FET parameters can be compared well to the FETs fabricated using PVD-grown electrodes with printed semiconductor (a-IGZO) layer.[24,26] Here, it is interesting to note that even though the printed ITO electrodes possess considerably

higher sheet resistance values (Figure S1) as compared to the sputtered ones, the all-printed FETs demonstrate attractive transistor characteristics that further improves with temperature.

Generally, the nitrate and acetate based metal precusrsors that are used to obtain IGZO precursor decomposes below 300 ºC and complete removal of any remaining organic residues takes place within the temperature range of 300-400 ºC. Therefore, this is the typically chosen temperature range for solution processed IGZO;[26,33–38] a further increase in annealing temperature increases the initial doping (free carrier) concentration, leaving the material conducting and resulting in depletion mode MOSFET behavior.[39,40] On the other hand, the carrier concentration at a particular annealing temperature also depends strongly on the relative ratio of In: Ga: Zn.[40] In general, solution processed IGZO is preferably annealed at 350 – 400 ºC for FET fabrication.[39] Therefore, when investigating the effect of two stage annealing, the IGZO layer has been annealed at 400 ºC.

The transfer and output characteristics for such two-steps annealed FETs are shown in Figures 3a and 3b, respectively. FET parameters for two-steps annealed device are extracted and compared with one-step annealed FET characteristics (Table 1). For the two-steps annealing process, the $I_{on/off}$, V_T and *SS* values are estimated to be as ~10^5, 0.37 V and 110 mV decade^{-1}, respectively. Next, in order to compare our all-printed device results with the standard practice, identical TFTs have also been prepared with sputtered ITO passives (Figure 3c-3f). In this case, the printed IGZO layer was annealed at both 400 ºC and 500 ºC, respectively. In accordance with previous reports, a high carrier doping, resulting in a strong negative shift of threshold voltage (around -0.5 V) has been observed when the annealing temperature was raised to 500 ºC.

In addition to $I_{on/off}$, V_T, and *SS*, the other most important parameter by which FET performance can be evaluated is device mobility (μ_{FET}). The μ_{FET} is considered to be the most important one to assess the quality of the semiconductor material and the semiconductor/

insulator interface. The μ_{FET} values of all the devices are calculated using the following equation;

$$\mu_{FET} = 2LI_{ds}/[WC_{dl}(V_{gs} - V_{th})^2] \quad (1)$$

where, L and W are the length and width of the channel; I_{DS} and C_{dl} are the drain current and the double layer capacitance of the electrolytic insulator at desired V_{GS} values (the value of gate voltage where the device mobility, μ_{FET}, is calculated), respectively. Here, all the parameters can be estimated using the FET's physical dimensions and electrical characteristics except C_{dl}. On the other hand, in case of electrolyte as gate insulator approach, the double layer capacitance value changes dramatically with continuous charge accumulation with the V_{GS} sweep. Therefore, a careful estimation of C_{dl} with respect to varying V_{GS} values is absolutely essential to estimate the device mobility accurately.

Although an electrolyte is used as the gate insulator, qualitatively the behavior of the metal-insulator-semiconductor capacitor (MISCAP) (composed of the gate electrode (ITO)/ electrolyte/ semiconducting a-IGZO) utilized in the present study compares well with the space charge density plots of metal-oxide-semiconductor field-effect transistors (MOSFETs). In the present study, the double layer capacitance (C_{dl}) of the a-IGZO/ electrolyte interface is calculated using cyclic voltammetry measurements on coplanar structures that are identical to the in-plane FET device geometry (Figure 4a). Figure 4b shows the cyclic voltammograms indicating the behavior of charging current as a function of the sweeping voltage at different scan rates. Current loops are observed to be closed but non-symmetric as can be expected for charge accumulation and depletion at the semiconductor interface. The sign of sweeping voltage is analogous to the gate voltage, and hence at positive sweeping voltage electrons accumulate at the a-IGZO surface and charging current increases. Electron depletion takes place in the opposite direction of sweep, a-IGZO being an n-type semiconductor, this results in a decrease in total surface charge density and a decrease in charging current. The current density (J) values are calculated using the overlapped area between CSPE and an a-IGZO

electrode for 0.5, 0.75, 1.0, 1.25 and 1.5 V applied sweeping voltages, which is plotted against different scan rates, as shown in Figure 4c. Interestingly, the current density versus scan speed plots are quite linear which can be taken as a proof of predominant capacitive coupling at the a-IGZO/ electrolyte interface; any slight deviation from the ideal scaling situation (current density should be proportional to dV/dt) can be due to little overlap of the electrolytic insulator with ITO contact pads (parasitic charging). The capacitance values at every applied potential can now be calculated using the slope of the current density versus scan rate plots and are found to be 0.78, 3.06, 4.89, 5.55 and 5.43 μF/cm^2 for 0.5, 0.75, 1.0, 1.25 and 1.5 applied sweeping voltages, respectively. These values are plotted as a function of different applied voltages showing a linear increase up to 1.0 V and then a somewhat saturation (Figure 4d), again typical behavior for a MISCAP device. Therefore, the identical co-planar structure used for the capacitance calculation provides an extremely realistic estimation of the double layer capacitance at every V_{GS} values and thus enable device mobility calculation at various gate voltages.

The variation of FET parameters (V_T, $I_{on/off}$, SS and μ_{FET}) for all-printed one-step, two-step annealed and sputtered ITO/ printed a-IGZO devices are summarized and compared in Table 1. From Table 1, it is evident that parameters like $I_{on/off}$ is identical for every alternate treatment that has been performed and adequate for logic operations; the value of SS hovers around 100 mV/dec, which ensures low voltage switching, and again found to be fairly independent of the various fabrication routines that we have excercized. However, there have been large spread in the imporatant performance parameter, field-effect mobility; the mobility values are found to be less than 10 cm^2/Vs, for any device, where the printed IGZO has been annealed at 400 ºC (in accordance with most of the publications involving solution processed IGZO, Table S1), higher performance has been recorded only for FETs annealed at 500 ºC. While, typically the amorphous oxides are not recommended to be annealed above 400 ºC, which results in very high carrier concentration and high negative threshold voltages. Here,

we find that our representive all-printed one-step annealed IGZO devices show a high mobility value (15.5 cm^2/Vs) without showing considerably high channel conductance at zero gate. This observation would later be explained based on the interfacial intermixing of components at the electrode/ channel interface. In contrast, the FETs prepared from sputtered ITO passives and annealed at 500 ºC show slightly higher mobility value than the one-step annealed diffused ITO/ a-IGZO interface devices, however, at the cost of high zero gate channel currents and a highly negative threshold voltage value. The high performance of our all-printed devices, which is easily among the best reported values for solution processed/ printed IGZO TFTs[33–36] is highly interesting given the fact that the printed ITO electrodes show orders of magnitude inferior conductivity as compared to the sputtered ITO passives. The comparable device mobility (with respect to standard sputtered passive FETs) coupled with near accumulation-mode device performance of our one step annealed all-printed FETs indicates that the physical, chemical and electronic compatibility of the semiconductor/ electrode interface must be playing an important role in deciding the device performance. Therefore, the investigation of the interface between S-D ITO electrodes and the a-IGZO channel is sought after.

Cross-sectional scanning electron microscopy (SEM) images of interface of one-step annealed (at 400 ºC), two-step annealed (first at 500 ºC and then at 400 ºC for IGZO) and sputtered ITO/ printed a-IGZO (annealed at 400 ºC) are shown in Figure 5a, b, and c, respectively. It is evident that in all-printed one-step and two-step annealed samples, a diffused interface between the a-IGZO and ITO passives can be noticed whereas a relatively sharp interface boundary is observed for the sputtered ITO/ printed a-IGZO sample. The diffusion at the interface in all-printed devices can be attributed to the physical compatibility resulting in superior intermixing in the respective oxide layers, as both the materials are solution processed. Here, one may correlate the electrical performance of the all-printed FETs with the diffusive nature of the a-IGZO/ ITO interface. Such diffused region often hampers

electronic transport; however, in this case, ITO and a-IGZO belong to the identical transparent oxide family; thus, intermixing at the interface may result in the restructuring/ reorganization among constituent elements leading to the electronically compatible region which may not actually reduce the semiconductor mobility, however, control the initial doping density, especially for high temperature annealed devices. In order to obtain a better resolution and complete insight of the elemental distribution in the diffused interface region, identical cross-sectional analysis is performed on all the samples using high-resolution transmission electron microscopy (HRTEM). The TEM results are found to corroborate the SEM observations; the all-printed devices show the diffused a-IGZO/ITO interface, marked by dashed rectangle (Figures S2a and S2b), however, the width of the diffused interface is found to be significantly smaller for all-printed two-step annealed sample, as compared to one-step annealed one. This is obvious as in the case of two-step heating, the intermixing and diffusion at the interface must be limited by the already crystalline ITO (through the first step of annealing). In contrast to these two instances, a sharp interface boundary in sputtered ITO/ printed a-IGZO (Figure S2c) indicates that there is no or very little interdiffusion taking place across the sputtered ITO interface. In addition, the formation of lattice fringes at ITO regions implies its crystalline nature in all three cases (Figure S2a, b, and c). At the next step, in order to investigate the distribution of the constituent elements, scanning transmission electron microscopy electron dispersive X-ray (STEM-EDX) mapping has been performed across the interface as shown Figure 5 (d-f). It is evident from the elemental maps that the constituents are present as per expectation, in the respective layers (In, Sn in ITO; In, Zn in a-IGZO), however, the distribution of Sn (Figure 5d, e and f, bottom panel, right) is found to be largely dependent on the fact whether both ITO and a-IGZO layers are printed and the necessary annealing process is carried out in one-step or in two-steps. Identical inter-diffusion behavior has also been observed by Kim *et al.* for the spin coated GaO and InZnO layers which at the end resulted in a complete intermixing and formation of IGZO semiconducting layer.[41] Here,

for the all-printed one-step annealed sample, the distribution of Sn is found to be in ITO, as well as within the a-IGZO layer across the interface (Figure 5d, bottom panel, right). This observation indicates that Sn from $In_{(1-x)}$-Sn_x-O (ITO layer) can easily diffuse into the amorphous In-Ga-Zn-O matrix (a-IGZO layer) while the other elements primarily remain in their respective layers. In comparison, the interlayer Sn diffusion is found to be insignificant for all-printed two-step annealed sample (Figure 5e, bottom panel, right), whereas, for the sputtered ITO and printed a-IGZO sample, Sn does not diffuse into the a-IGZO layer at all (Figure 5f, bottom panel, right).

Here, it is important to note that the diffusion of Sn from ITO to a-IGZO in all-printed devices may lead to a change in the electronic environment across the interface; therefore, it is necessary to investigate the electronic structure of a-IGZO/ ITO interface. Consequently, qualitative as well as quantitative studies are performed using the photoelectron spectroscopy measurements on the one-step annealed a-IGZO/ ITO sample. The core level spectra of constituents (In, Sn, Ga, and Zn) for ITO, a-IGZO, and a-IGZO/ ITO is shown in Figure S3 which do not show a significant shift from one sample to another except slight shift of In and Ga peaks towards lower binding energy for a-IGZO/ ITO sample. Oxygen spectral peak (O 1S) which usually deconvolutes into three nearly Gaussian peaks, contains the information of its contributions to bond with metallic ions (529.5 eV), vacancies (530.5 eV) and adsorbed species such as -CO_3, -OH etc. (532.5 eV).[42,43] The deconvoluted peaks, their corresponding centers and areas (%) for ITO, a-IGZO and a-IGZO/ ITO interfacial region is shown in Figure 6a, b, and c, respectively. Here, it is evident that a-IGZO top surface is more favorable for external loosely adsorbed oxygen species as compared to ITO. It is probably due to the presence of Zn in a-IGZO which has more affinity to oxygen.[44] The a-IGZO/ ITO interface shows the intermediate result of a-IGZO and ITO alone for these adsorbed species. In addition to core levels spectra, depth profiling and ultraviolet photoelectron spectroscopy (UPS) studies have been carried out to obtain a closer look at the interface and the band structure

information. The depth profiling of a-IGZO/ ITO indicates that initially In, Ga and Zn core levels appeared, however, with further depth profiling (towards the interface), Sn feature also starts to appear along with In, Ga, and Zn (see Table S2). The content of In and Zn does not change significantly at further deep inside the interface, however, relatively small but a noticeable decrease in Ga and an increase in Sn can be observed. Here, we are expecting that low ionic radius of Sn makes it suitable to sit onto the Ga sites in the amorphous In-Ga-Zn-O matrix by replacing the Ga atoms. Furthermore, the shift of Ga binding energy towards lower side (breaking the oxidation of Ga) with depth profiling of the a-IGZO/ ITO interfacial region corroborates this argument. The substitution of Sn at Ga site leads to the formation of In-Sn-Zn-O (ITZO) locally which provides the extra electron and, thus, the formation of more conducting ITZO at the interface. Figure 6d, e, and f show the UPS spectra for ITO, a-IGZO and at a-IGZO/ ITO interface region where Sn starts to appear after depth profiling. The position of the valence band maxima is estimated using tangent at the onset of photoemission (see Figure S4) with respect to the Fermi level (E_F) and the values of work function are estimated as a difference between incident energy (He-I, 21.22 eV) and the secondary cutoff. These estimated values are shown in the proposed schematic band diagram, (Inset of Figure 6 (d-f)). At a-IGZO/ ITO interface, the difference between the work functions (0.75 eV) of both materials may lead to high barrier height with the subject to the alignment of E_F. While in case of ITZO/ ITO interface, the difference reduces down to 0.29 eV, and thus, the barrier height decreases significantly (Figure S5). In other words, this intermediate layer of ITZO, between the ITO electrode and the a-IGZO semiconductor layer offers excellent band alignment all the way across the interface; the interlayer work function difference is never too high, i.e. a large band bending is never required. On one hand, this ensures easy carrier transport across the intermediate layer, which enables near Ohmic contact and high carrier mobility, on the other hand, the diffused layer controls the the carrier concentration and channel conductance.

At the next level, the all-printed FETs are integrated together to fabricate simple logic units; various n-MOS based unipolar inverters with different types of loads, such as, a resistor (R-mode), an enhancement type n-MOS (E-mode) and a depletion type n-MOS (D-mode), as shown schematically in Figure 7a. Initially, the inverter circuits are constructed with sputtered ITO electrodes in order to figure out the most suitable load and then it is reproduced with the all-printed FETs. For all these fabricated inverter circuits, the channel (50 μm, for both drive and load FETs) and the number of printing pass for a-IGZO (2 layers, leading to 70 nm thickness) are kept constant. Figure 7b shows the input-output characteristics of fabricated inverters along with their signal gain profiles for sputtered ITO and printed a-IGZO in R-mode, E-mode and D-mode configurations, respectively with a drive voltage of V_{DD} = 0.5 V. Typically, inverter performance is characterized by its signal gain value (gain= dV_{out}/dV_{in}). However, in the case of unipolar inverters, the signal gain is not only determined by the performance of the drive FET but also by the load characteristics (see Figure S6). Here, the inverters fabricated with sputtered ITO and printed a-IGZO show the signal gain values of 2.6, 0.9 and 3.0 for R-mode (1 MΩ), E-mode and D-mode devices, respectively, at V_{DD} = 0.5 V, indicating that D-mode load is most suitable. At the next step, the all-printed inverter circuit is fabricated by employing one-step heating process at 500 °C with the D-mode load. The input-output characteristic is shown in Figure 7c; here a signal gain of 2.5 is obtained for V_{DD} = 0.5 V. The signal gain value in present work is not significant but comparatively superior to earlier reported solution process oxide of similar configuration.[45–47] Figure 7d shows a comparison of signal gain values for sputtered ITO and all-printed inverters for varying input signal values. It is believed that a more careful optimization of the selected load profile with respect to the device characteristic of the drive FETs can certainly improve the performance of these all-printed inverters.

■ CONCLUSIONS

Oxides based electrolyte-gated, all-printed FETs and logic inverters are successfully demonstrated here in this study, which show performances comparable to the devices that are fabricated using lithographically patterned and sputtered ITO electrodes. The excellent device characteristics of the all-printed FETs, even with an inferior electrode quality, can be attributed to the formation of diffused a-IGZO/ ITO interfaces, which allows annealing at higher temperatures without rendering the zero gate channel conductance too high. The cross-sectional microscopic studies clearly identify the diffused regions at the interface, where Sn from ITO layer is found to get substituted at the Ga site in IGZO phase and the XPS investigations reveal that the reorganization of constituent elements at the atomic level leads to a diffused variation of Fermi level at the interface. In other words, an excellent band alignment from the electrode to the intermediate Sn-rich IGZO layer (or a-ITZO) and the said a-ITZO layer to the semiconducting a-IGZO layer exist, which, in turn, results in excellent near Ohmic contacts, high carrier mobility and controlled channel conductance upon annealing at higher temperatures. Undoubtedly, the selection of the electrode and semiconductor materials, stemming from identical material family, has facilitated the diffused interface formation and excellent band alignment. It may be concluded here that the present findings and the scientific understanding acquired in this study, which are also well supported by the comprehensive microscopic and spectroscopic measurements we have performed, may actuallygo beyond the scope of printed electronics.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI:

Experimental details, Table S1 for comparing our results with earlier reported work, Table S2, Sheet resistance data, HR-TEM cross-sectional images, XPS data, Scheme of band diagram, Scheme of output and load ckaracterstics for inverter, References.

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Notes

The authors declare no competing financial interest.

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Table 1. FET parameters such as $I_{on/off}$, V_{th}, SS, and μ at are tabulated for all the devices that are fabricated using different processing schemes and annealing treatments.
(AP: All-Printed, S+P: Sputtered electrodes along with printed semiconductor; the associated number indicates the annealing temperature)

Sample	$I_{on/off}$ **(**V_{GS} **= 1.0)**	V_T **(V)**	**SS**	**μ at** V_{GS} **= 1.0 (**$cm^2/V \cdot s$**)**
AP-400	$6x10^4$	0.01	90	0.46
AP-450	$7x10^5$	-0.12	100	2.4
AP-500	$2x10^5$	-0.16	110	15.5
AP-(500+400)	$2x10^5$	0.37	110	5
S+P-(400)	$1x10^7$	-0.08	100	2.9
S+P-(500)	$1x10^5$	-0.46	184	22.7

Figure Captions

Figure 1. (a) The schematic representations of complete FET fabrication steps in a sequential manner. (b) and (c) XRD patterns of ITO and a-IGZO films, respectively, for different annealing temperatures. (d) and (e) AFM images of printed ITO and a-IGZO layers, respectively, annealed at 400 °C.

Figure 2. Transfer and output characteristics of all-printed FETs with one-step heating at (a) and (b) 400 °C, (c) and (d) 450 °C, (e) and (f) 500 °C, respectively, at V_{ds} 1.0 V. Out-put characteristics are shown at different V_{gs}.

Figure 3. Transfer and output characteristics of (a) and (b) all-printed FET with two-steps heating at 500 °C for ITO and 400 °C for a-IGZO, (c) and (d) FET with sputtered ITO and printed a-IGZO annealed at 400 °C at V_{ds} 1.0 V, (e) and (f) FET with sputtered ITO and printed a-IGZO annealed at 500 °C at V_{ds} 1.0 V. Out-put characteristics are shown at different V_{gs}.

Figure 4. (a) Schematic representations of an in-plane capacitor with ITO and a-IGZO working electrodes (WE). (b) Charging current loops as a function of a potential sweep at different scan rates in mV per second scale (mVps). (c) Variation of current density (J) as a function of scan rates at different applied potentials. (d) Variation of calculated capacitance values for different applied potentials.

Figure 5. Cross-sectional SEM images of a-IGZO-ITO interface for (a) all-printed one-step annealed, (b) all-printed two-step annealed and (c) sputtered ITO with printed a-IGZO FETs. (d), (e) and (f) show STEM cross-sectional view (top left) of mapped layers (indicated by rectangle) with scale bars 500, 100 and 100 nm and the STEM-EDX elemental maps indicating the diffusion distributions of In, Zn and Sn elements (top right and bottom two panels) for all-printed one-step, two-steps and sputtered ITO with printed a-IGZO, respectively.

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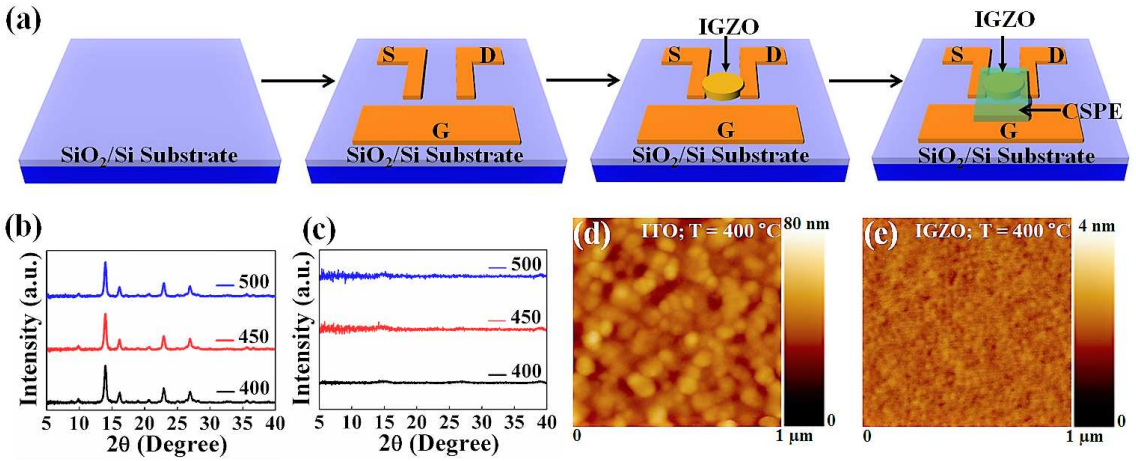

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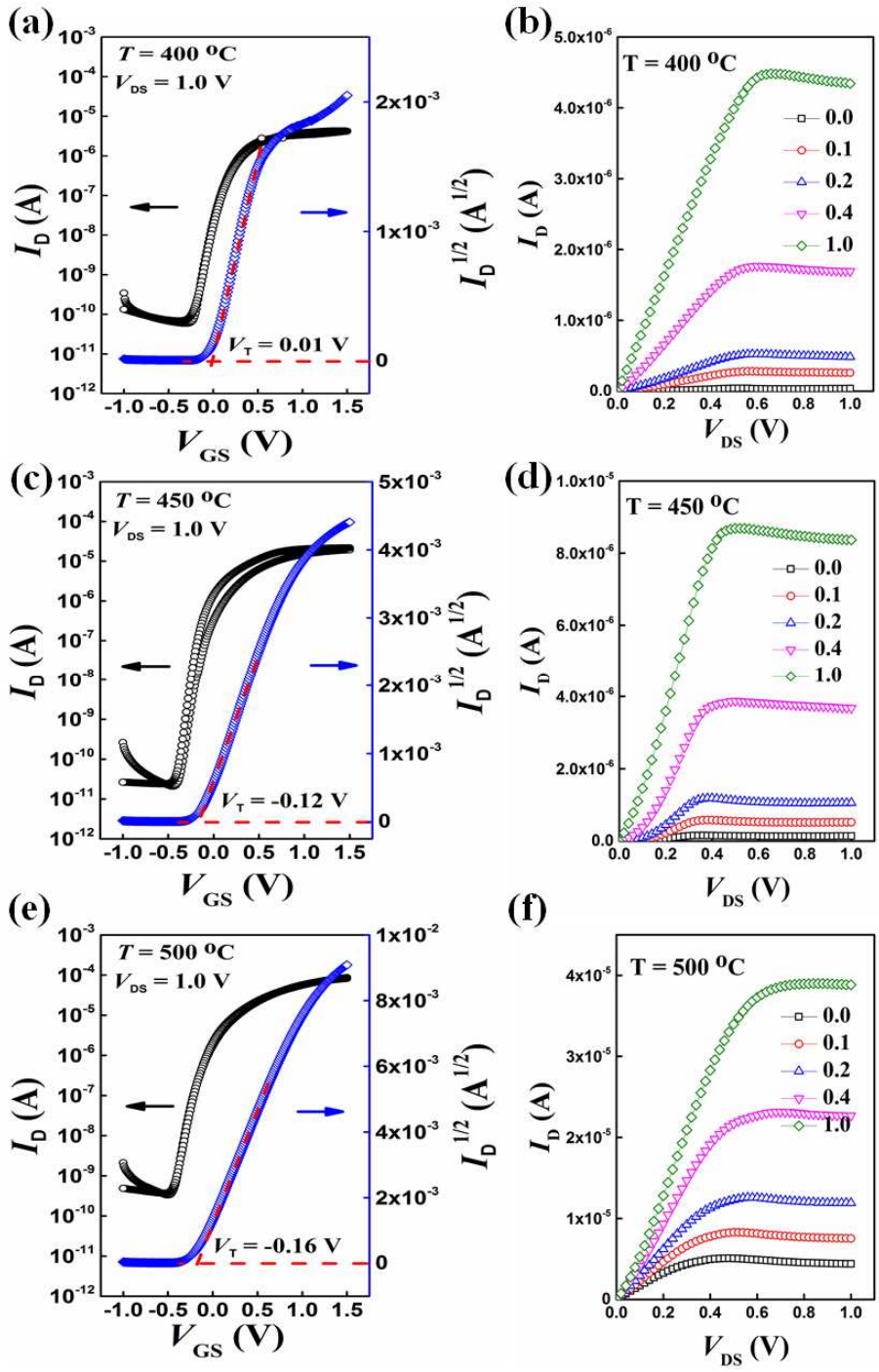

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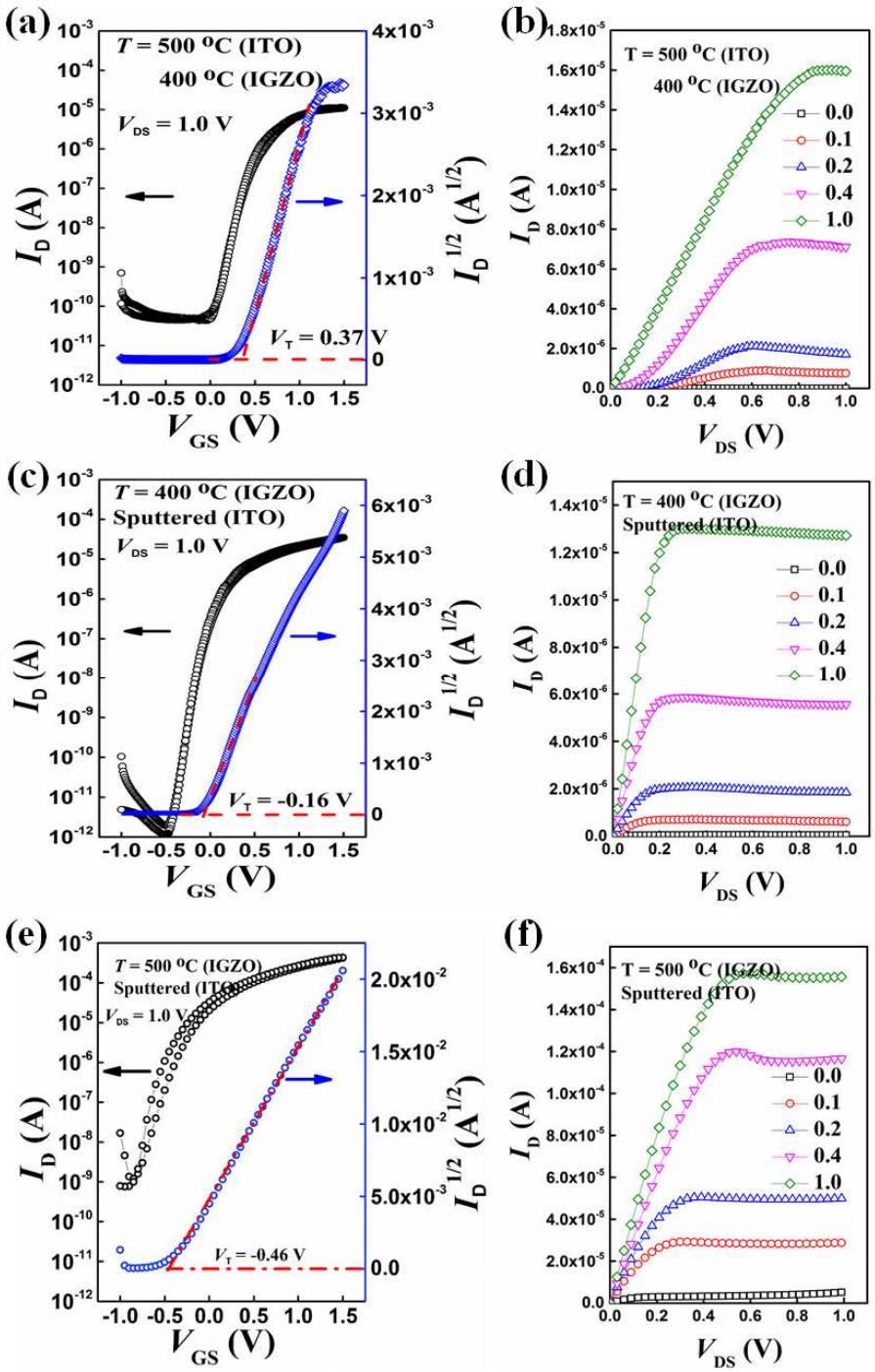

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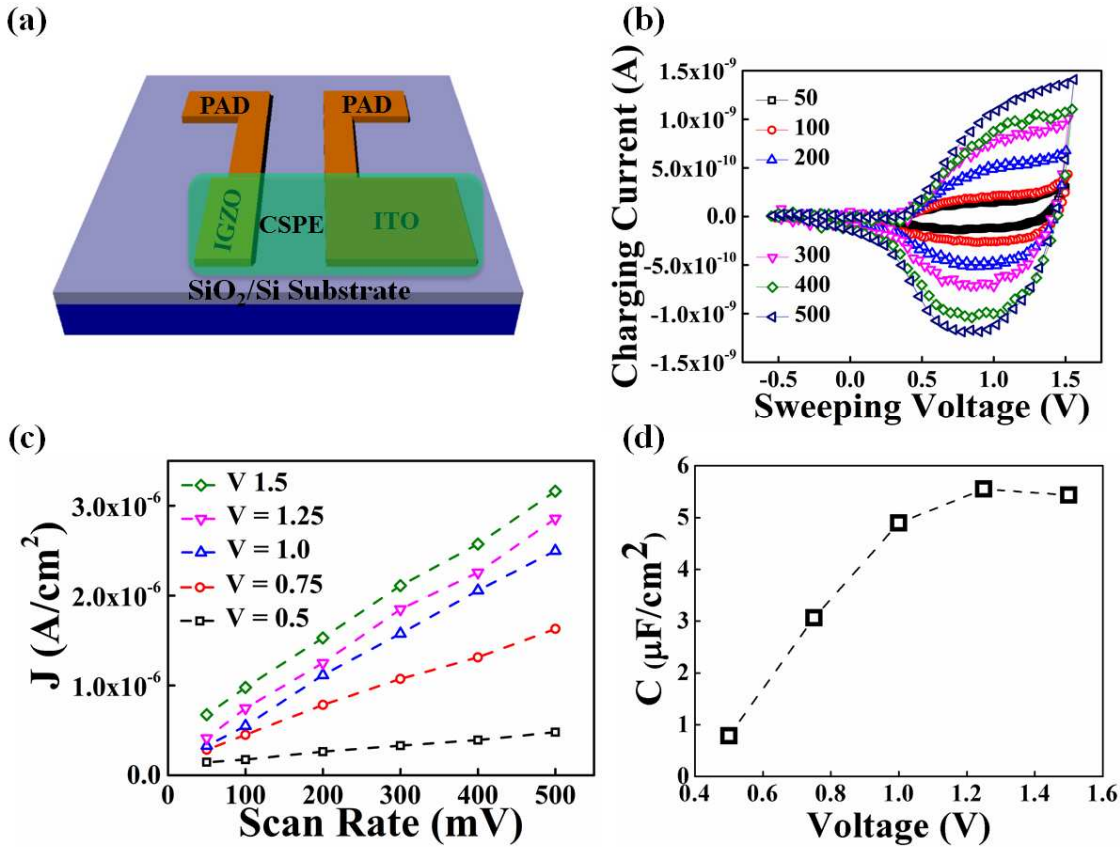

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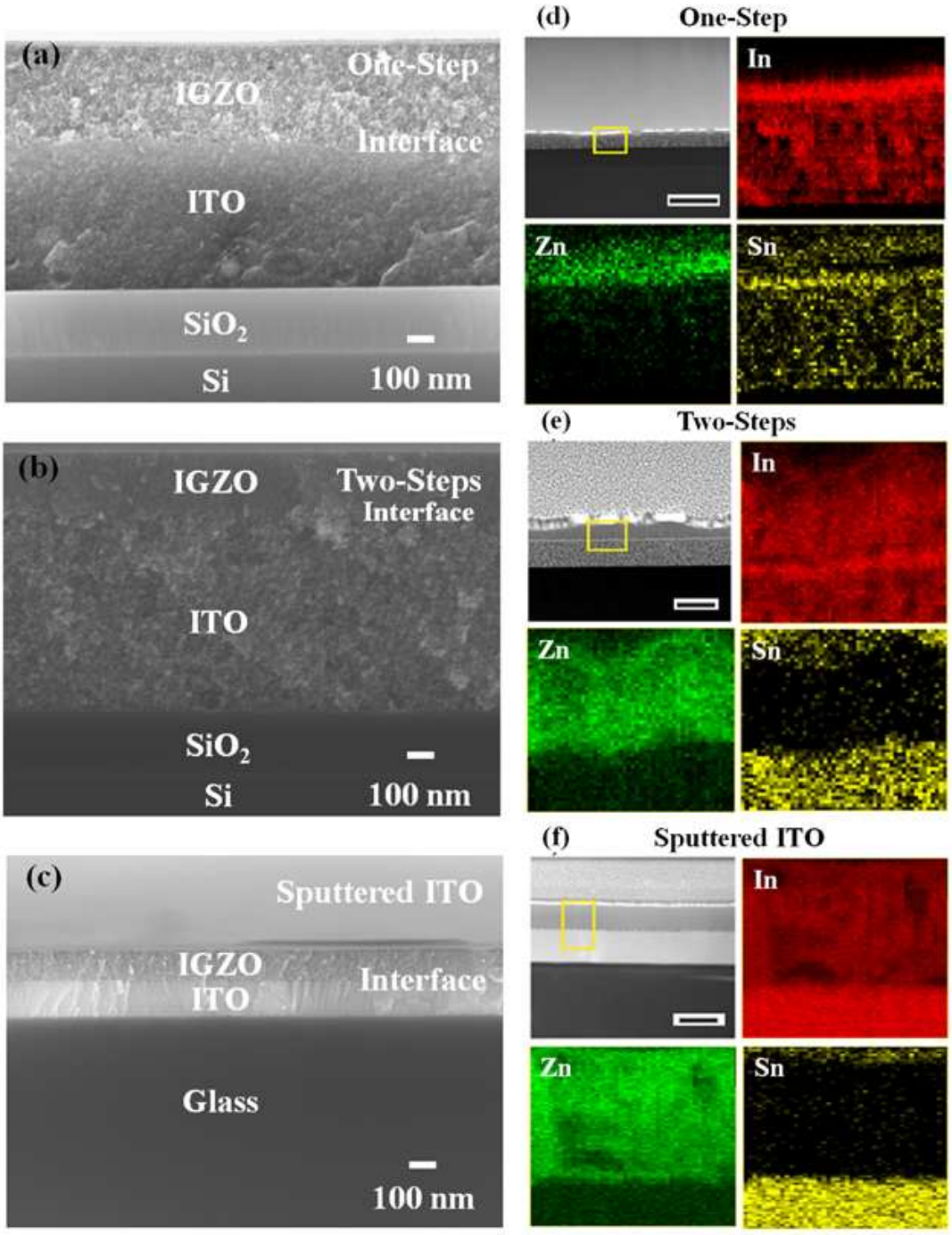

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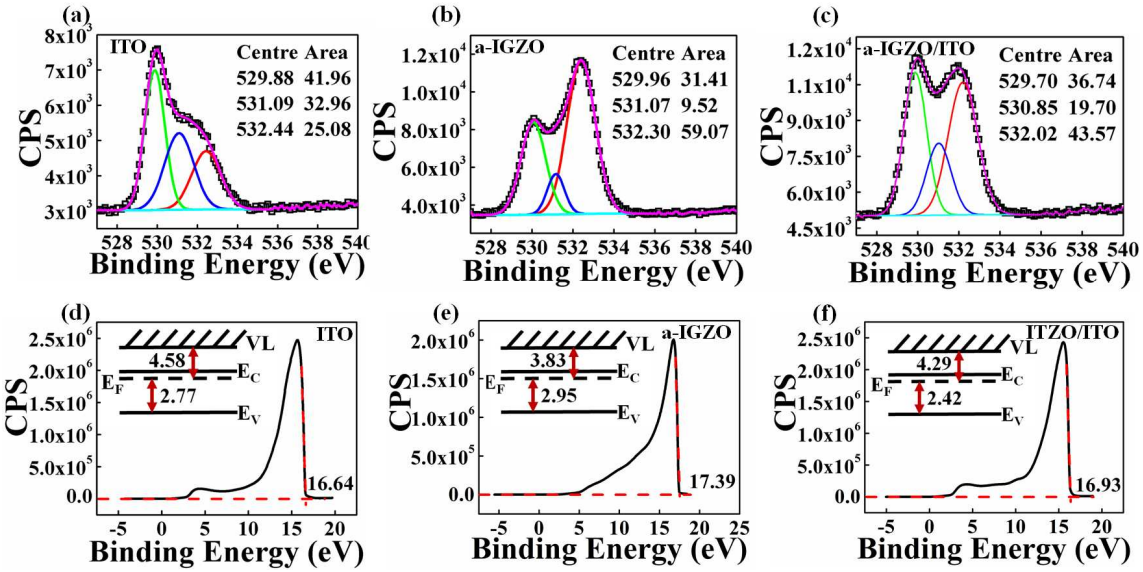

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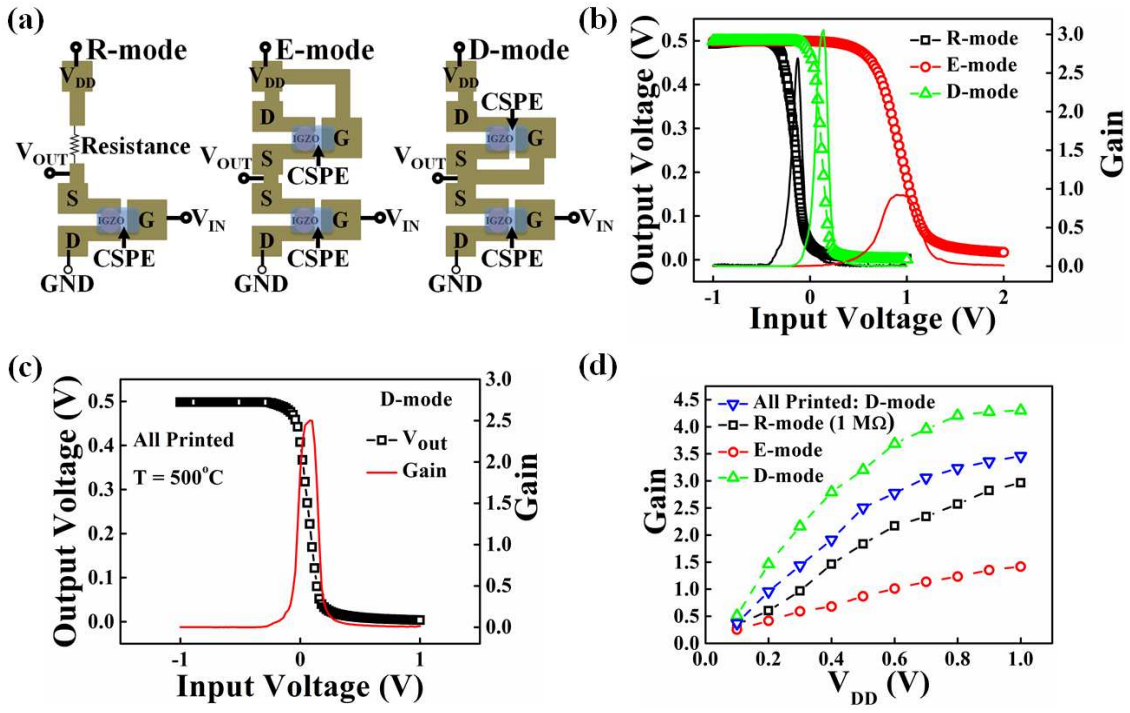

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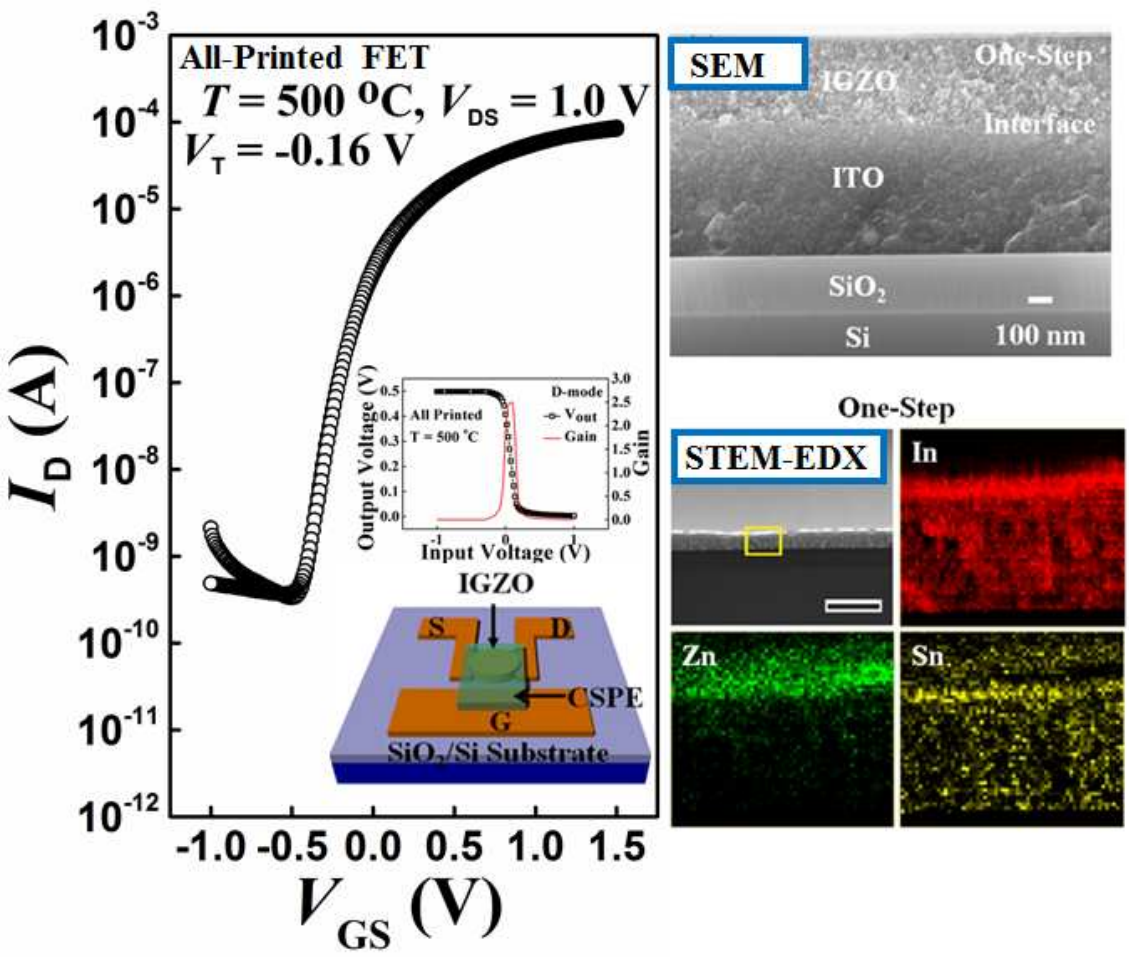
TOC


All-Printed FET
T = 500 °C, V_DS = 1.0 V
V_T = -0.16 V
I_D (A)
V_GS (V)
All Printed
T = 500 °C
D-mode
Vout
Gain
Output Voltage (V)
Input Voltage (V)
IGZO
S
D
G
CSPE
SiO2/Si Substrate
SEM
IGZO
One-Step
Interface
ITO
SiO2
Si
100 nm
One-Step
STEM-EDX
In
Zn
Sn